APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV	DESCRIPTION	DATE	APPROVED
		A	ECO 302: INPUT POWER	6/18/09	JWM

CONTRACT NO.		QUAD TRON, INC.				
APPROVALS	**DATE**	**PCM ENCODER, MODEL PCM2-RS422+MOD**				
DRAWN MJC	6/9/09					
CHECKED RHM	6/9/09	SIZE	FSCM NO.	DRAWING NO.		REV A
ISSUE JWM	6/9/09	**A**	**OBPE4**	**57-2638**	SHEET 1 OF 9	

MODEL PCM2-RS422+MOD

PCM Encoder Operation Parameters:

Bit Rate: Programmable, DC to 5 mega bits per second.

Bits Per Word: 8, 9, 10, 11, 12, 13, 14, 15, 16, programmable.

Synchronization Pattern:
Synchronization pattern and sub-frame ID's are programmable.

Frame Format:
Any frame format is programmable with sub frames and super commutation allowed. A counter may also be programmed within the frame format along with a sub-frame ID counter.

PCM Code Outputs:
Single Ended PCM output 1
RS422 PCM output 1
RS422 PCM output 2
RS422 PCM output 3

The PCM code output is programmable to the following codes:

NRZ-L	BIO-L	
NRZ-M	BIO-M	RNRZ-L (randomized data)
NRZ-S	BIO-S	

Other Outputs:
Bit Clk; Word Pulse; Frame Pulse; Sync Pulse.

Asynchronous Data Input:
2 Channels Asynchronous Data Input for PCM data acquisition.

Power Requirements: +28Vdc, ±4Vdc at 225 mA Nominal.

Input Power: (B+ , B+ RTN) is isolated from DGND; CHASSIS GND and all equipment signals.

Voltage Protection: ±35 Vdc will not damage the unit.

PRE MODULATION FILTER:
Housing connector and mounting slot for the Quad Tron Model, PMF9-LD.

RS422 ASYNC MODULE

CA_RS422 Module Description

The CA_RS422 Module implements six channels of asynchronous RS422 data reception. Each channel contains an RS422 receiver, followed by a UART, followed by a 1K word deep by 16 bit wide RAM FIFO. The user programs the PCM frame format to insert FIFO output words into the PCM data stream. The user programs the PCM word size from 4 to 16 bits. If the PCM word size is less than 16 bits, then the LSB's of the FIFO data word are truncated to equal the PCM word size. The user programs the PCM bit rate.

At the front connector, a clear to send (CTS) signal for each of the 6 channels is available. CTS=1 indicates the FIFO is not full. Each of the six channels received character is echoed in RS422 format at the front connector for debug purposes (there are 6 separate RS422 transmitters available).

The 16 bit FIFO word format is shown below:

MSB							LSB
of bits	# of bits [	5 to 9,	1,	1,	1,	1,	1,	2 to 5]

MSB [UART CHARACTER, FIFO BUFFER UNDERFLOW, FIFO BUFFER OVERFLOW, UART PARITY ERROR, UART FRAMING ERROR, UART DATA OVERRUN ERROR, ZERO FILL] LSB

The CA_RS422 Module can also be programmed to output FIFO words with the UART error bits logical or'ed for shorter PCM word sizes. This 16 bit FIFO word format is shown below:

MSB					LSB
# of bits [	5 to 9,	1,	1,	1,	5 to 8]

MSB [UART CHARACTER, FIFO BUFFER UNDERFLOW, FIFO BUFFER OVERFLOW, UART ERROR, ZERO FILL] LSB

UART CHARACTER: Can be 5, 6, 7, 8, or 9 bits. These bits are left justified with the BAUD MSB positioned at the FIFO word MSB.

FIFO BUFFER UNDERFLOW: This bit=1 indicates that the FIFO buffer is empty and the FIFO word is a repeat of the previous FIFO word.

FIFO BUFFER OVERFLOW: This bit=1 indicates that the FIFO buffer overflowed. This indicates that the UART data is being put into the FIFO at a faster rate than it is being taken out. To prevent this situation, the user should increase the PCM bit rate, change the PCM frame format or decrease the rate at which data is being put into the FIFO.

UART PARITY ERROR: See UART description.

UART FRAMING ERROR: See UART description.

UART DATA OVERRUN ERROR: See UART description.

UART ERROR: Set=1 if any of the 3 possible UART errors occurred.

ZERO FILL: Zero fill LSB's to obtain a 16 bit FIFO word size.

UART Description

Features:

- High Resolution Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8 or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and parity check Supported by Hardware
- Data OverRun Detection
  Framing Error Detection

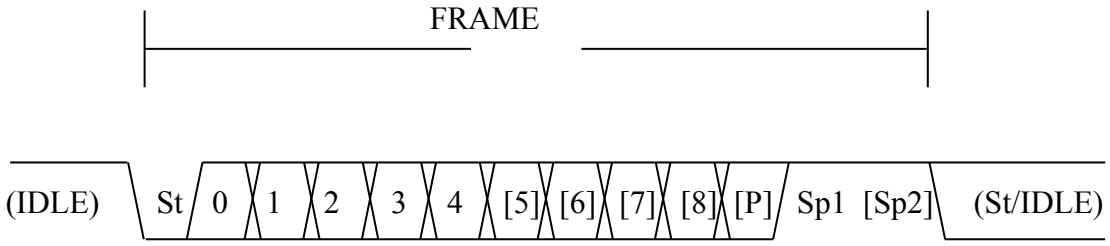
Frame Formats:

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits), and optionally a parity bit for error checking. The UART accepts all 30 combinations of the following as valid frame formats:

- 1 start bit
- 5, 6, 7, 8, or 9 data bits
- no, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the start bit followed by the least significant data bit. Then the next data bits, up to a total of nine, are succeeding, ending with the most significant bit. If enabled, the parity bit is inserted after the data bits, before the stop bits. When a complete frame is transmitted, it can be directly followed by a new frame, or the communication line can be set to an idle (high) state. Figure 1 illustrates the possible combinations of the frame formats. Bits inside brackets are optional.

Figure 1. Frame Formats



St	Start bit, always low.
(n)	Data bits (0 to 8).
P	Parity bit. Can be odd or even.
Sp	Stop bit, always high.
IDLE	No transfers on the communication line (RxD or TxD). An IDLE line must be high.

Parity Bit Calculation:

The parity bit is calculated by doing an exclusive-or of all the data bits. If odd parity is used, the result of the exclusive or is inverted. The relation between the parity bit and data bits is as follows:

$P_{even} = d_{n-1} \oplus ... \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 0$

$P_{odd} = d_{n-1} \oplus ... \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 1$

P_{even} Parity bit using even parity
P_{odd} Parity bit using odd parity
d_n Data bit n of the character

If used, the parity bit is located between the last data bit and first stop bit of a serial frame.

Receiver Error Flags:

The UART receiver has three error flags: Frame Error, Data OverRun, and Parity Error.

The Frame Error (FE) flag indicates the state of the stop bit. The FE flag is zero when the stop bit was correctly read (as one), and the FE flag will be one when the stop bit was incorrect (zero). This flag can be used for detecting out-of-sync conditions, detecting break conditions and protocol handling.

The data OverRun (DOR) flag indicates data loss due to UART receiver buffer full condition. A data overrun occurs when the UART receive buffer is full (two characters), there is a new character waiting in the Receive Shift Register, and a new start bit is detected. If the DOR flag is set there was one or more charaters.

The Parity Error (UPE) flag indicates that the character has a parity error when received zero.

Baud Rates:

Table 2. Examples of UBRR Settings for Commonly Used Oscillator Frequencies

Baud Rate (bps)	f_{osc} = 7.3728 MHz	
	U2X = 0	U2X = 1
	Error	Error
2400	0.0%	0.0%
4800	0.0%	0.0%
7200	0.0%	0.0%
9600	0.0%	0.0%
14.4k	0.0%	0.0%
19.2k	0.0%	0.0%
28.8k	0.0%	0.0%
38.4k	0.0%	0.0%
57.6k	0.0%	0.0%
76.8k	0.0%	0.0%
115.2k	0.0%	0.0%
230.4k	0.0%	0.0%
460.8k	0.0%	0.0%
921.6k	0.0%	0.0%
Max (1)	460.8kbps	921.6kbps

1. UBRR = 0, Error = 0.0%

Other Baud Rates can be obtained by using the following formula in Table 2.

Table 2. Equations for Calculating Baud Rate Register Setting

Operating Mode	Equations for Calculating Baud Rate (1)
U2X = 0	$BAUD = \frac{f_{osc}}{16 (UBRR + 1)}$
U2X = 1	$BAUD = \frac{f_{osc}}{8 (UBRR + 1)}$

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Note: 1. The baud rate is defined to be the transfer rate in bit per second (bps).

BAUD Baud Rate (in bits per second, bps)
f_{osc} System Oscillator clock frequency, standard is 7.3728 MHz.
UBRR Contents of the UBRRH and UBRRL Registers, (0-4095), set by the user.

EMC QUALIFICATIONS:

STANAG 3516 AE (Edition 5): Electromagnetic interference, Test methods for aircraft Electrical and Electronic Equipment.

MIL-STD-461E: Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment's.

NT-UB-MAK-07001 ISSUE A: B2 EMC Equipment Requirements.

ENVIRONMENTAL QUALIFICATIONS:

MIL-STD-810 MILITARY STANDARD ENVIRONMENTAL TEST METHODS.

NT-U-MAK-07002, B2 ENVIRONMENTAL EQUIPMENT REQUIREMENTS, Rev. C

Standard Environmental:

Operating Temperature:	-40°C to +85°C
Storage Temperature:	-55°C to +125°C
Humidity:	Relative humidity of 85% for two hours at 65°C.
Altitude:	Unlimited
Vibration:	20g's RMS from 5 to 2000Hz in each major axis.
Acceleration:	Constant acceleration of 100g's in each axis.
Shock:	100g's for 10m second in each major axis.

Mechanical: Outline Drawing: 48-2537

Engraving: PCM2-RS422
PCM2-DIGN
PCM2-PS

PCM2 BASE MODULE, J1 CONNECTOR
J1 CONNECTOR, MDM-51S

SIGNAL NAME	PIN
BI0	1
BI1	2
BI2	3
BI3	4
BI4	5
BI5	6
BI6	7
BI7	8
BI8	9
BI9	10
BI10	11
BI11	12
CODE2_422-	13
CODE2_422+	14
CODE4_422-	15
CODE4_422+	16
RESERVED	17
CHASSIS GND	18
BITCLK	19
CODE1	20
BI12	21
BI13	22
BI14	23
BI15	24
BI16	25

SIGNAL NAME	PIN
BI17	26
BI18	27
BI19	28
BI20	29
BI21	30
BI22	31
BI23	32
DGND	33
DGND	34
RESERVED	35
DGND	36
R232	37
T232	38
FRAME_PLS	39
WORD_PLS	40
SYNC_PLS_422-	41
SYNSC_PLS_422+	42
CODE3_422-	43
CODE3_422+	44
B+	45
B+	46
B+	47
B+RTN	49
B+RTN	50
B+RTN	51

RS422 MODULE, J1 CONNECTOR
J1 CONNECTOR, MDM37S

SIGNAL	PIN
IN1_RS422+	31
IN1_RS422-	12
IN2_RS422+	18
IN2_RS422-	17
IN3_RS422+	4
IN3_RS422-	3
IN4_RS422+	23
IN4_RS422-	22
IN5_RS422+	2
IN5_RS422-	1
IN6_RS422+	21
IN6_RS422-	20
CTS1	5
CTS3	6
CTS5	7
CTS2	24
CTS4	25
CTS6	26
OUT1_RS422+	14
OUT1_RS422-	13
OUT2_RS422+	15
OUT2_RS422-	16
OUT3_RS422+	10
OUT3_RS422-	29
OUT4_RS422+	30
OUT4_RS422-	11

SIGNAL	PIN
OUT5_RS422+	28
OUT5_RS422-	9
OUT6_RS422+	8
OUT6_RS422-	27
CARD_STRAP0	32
CARD_STRAP1	33
CARD_STRAP2	34
CARD_STRAP3	35
CARD_STRAP4	36
GND	19
GND	37